IN THE CLAIMS

Please amend the claims as follows:

1. - 22. (Cancelled)

23. (Original) A synchronizer unit comprising:

a first synchronizer unit to receive a plurality of clock signals and a reset signal and to generate a synchronized reset signal;

a second synchronizer unit to receive the plurality of clock signals and the synchronized reset signal and to generate a plurality of write reset signals; and

a third synchronizer unit to receive a sample clock signal, the synchronized reset signal, and the plurality of write reset signals and to generate a read reset signal having a latency with respect to each of the write reset signals of less than or equal to one clock cycle.

24. (Original) The synchronizer unit of claim 23, wherein the first synchronizer unit comprises a plurality of clock signal paths, wherein each of the plurality of clock signal paths comprises a plurality of serially connected flip-flops.

25. (Original) The synchronizer unit of claim 24, further comprising an OR gate coupled to each of the plurality of clock signal paths, the OR gate having an output node providing the synchronized reset signal.

26. (Original) The synchronizer unit of claim 24, wherein the second synchronizer unit comprises a plurality of clock signal paths, wherein each of the plurality of clock signal paths comprises a plurality of serially connected flip-flops.

27. (Cancelled)

28. (Previously Presented) A method of forming a read reset signal, the method comprising:

synchronizing a first reset signal to a plurality of clock signals to form a synchronized reset signal;

synchronizing the synchronized reset signal to the plurality of clock signals to form a plurality of write reset signals; and

synchronizing the synchronized reset signal to a sample clock signal to form a read reset signal having a latency with respect to each of the plurality of write reset signals of less than or equal to one clock cycle, wherein synchronizing a first reset signal to a plurality of clock signals to form a synchronized reset signal comprises:

clocking the first reset signal into a plurality of parallel flip-flops using the plurality of clock signals to clock each of the plurality of parallel flip-flops to form a plurality of clocked reset signals; and

ORing the plurality of clocked reset signals to form the synchronized reset signal.

29. (Previously Presented) A method of forming a read reset signal, the method comprising:

synchronizing a first reset signal to a plurality of clock signals to form a synchronized reset signal;

synchronizing the synchronized reset signal to the plurality of clock signals to form a plurality of write reset signals; and

synchronizing the synchronized reset signal to a sample clock signal to form a read reset signal having a latency with respect to each of the plurality of write reset signals of less than or equal to one clock cycle, wherein synchronizing the synchronized reset signal to the plurality of clock signals to form a plurality of write reset signals comprises:

clocking the synchronized reset signal into a plurality of parallel flip-flops using the plurality of clock signals to clock each of the plurality of parallel flip-flops to form the plurality of write reset signals.

30. (Previously Presented) A method of forming a read reset signal, the method comprising:

synchronizing a first reset signal to a plurality of clock signals to form a synchronized reset signal;

synchronizing the synchronized reset signal to the plurality of clock signals to form a plurality of write reset signals; and

synchronizing the synchronized reset signal to a sample clock signal to form a read reset signal having a latency with respect to each of the plurality of write reset signals of less than or equal to one clock cycle, wherein synchronizing the synchronized reset signal to a sample clock signal to form a read reset signal having a latency with respect to each of the plurality of write reset signals of less than or equal to one clock cycle comprises:

adjusting a number of flip-flops in a signal path such that the read reset signal with respect to each of the plurality of write signals has a latency of less than or equal to one clock cycle.